III. **AMENDMENTS TO THE CLAIMS**

The following is a listing of claims to replace all prior versions and listings of claims in the application:

1. (Currently Amended) An error correcting logic system comprising:

at least two redundant dynamic logic gates, each dynamic logic gate outputting one of a first logic state and a second logic state, the second logic state being output in response to a logic input signal; and

an interconnecting gate coupled to an output of each redundant dynamic logic gate, the interconnecting gate outputting the second logic state only when all of the redundant logic gates output the second logic state,

wherein the interconnecting gate includes a NOR gate;

wherein each dynamic logic gate includes a combinatorial logic section and a pre-charge section having a pre-charge device and a keeper device;

wherein an output of the NOR gate feeds back to the keeper device.

2. (Original) The system of claim 1, wherein the interconnecting gate includes an AND gate.

3. (Original) The system of claim 2, wherein the AND gate includes a NAND gate coupled to an inverting gate.

4. (Original) The system of claim 2, wherein each dynamic logic gate includes a combinatorial logic section, a pre-charge section, and an inverting gate positioned downstream of a node

connecting the combinatorial logic section and the pre-charge section.

5. (Original) The system of claim 4, wherein the pre-charge section includes a pre-charge device and a keeper device.

6. (Original) The system of claim 5, wherein an output of the inverting gate feeds back to the keeper device.

7. – 9. (Cancelled)

10. (Original) The system of claim 1, wherein the fault is a negative fault.

11. (Original) The system of claim 1, wherein the interconnecting gate is a static gate.

12. (Original) The system of claim 1,wherein each dynamic logic gate is a cascode voltage switch.

13. – 20. (Cancelled)